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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,150	MATSUDA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 17-40 have been considered but are moot in view of the new ground(s) of rejection.

In addition, revision to previous rejections address any of the Applicant's arguments in the Response filed 05/27/2008.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 17, 18, 22, 23, 27, 28, 32 and 33 recite, "configuring erasure position information"… "of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data **before being deinterleaved**". There is no antecedent basis anywhere in the specification for such language as highlighted and underlined.

The amendment filed 05/27/2008 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: Claims 17, 18, 22, 23, 27, 28, 32 and 33 recite, "configuring erasure position information"... "of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data **before being deinterleaved**". The language as highlighted and underlined is new matter.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Objections

Claims 19, 24, 37 and 38 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 19, 24, 37 and 38 fail to recite any positive limitation further limiting the error correction methods of claims 18 and 23. Claims 19, 24, 37 and 38 instead recite the intended use of the error correction methods of claims 18 and 23 on data comprising sync data

without reciting any positive limitation in the form of a step describing how the sync data is used further narrowing the error correction methods of claims 18 and 23.

Claims 29-31, 39, 34-36 and 40 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function, because apparatus claims cover what a device is, not what a device does (Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). Claims 29-31, 39, 34-36 and 40 fail to recite any structural element and/or structural interconnections explicitly relating the "nonfunctional descriptive material" and/or functional language in claims 29-31, 39, 34-36 and 40 to the error correction apparatus of claims 28 and 33.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 17-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 17, 18, 22, 23, 27, 28, 32 and 33 recite, "configuring erasure position information"... "of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data **before being deinterleaved**". The language as highlighted and underlined is new matter.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18, 19, 23, 24, 37 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Claims 18 and 23 recite, "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second

byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block". The previous quoted recitation is "nonfunctional descriptive material" describing a data structure used in the data storage environment for which the error correction methods of claims 18 and 23 is intended to be applicable. Claims 18 and 23 fail to recite any functional steps of a method explicitly relating the quoted "nonfunctional descriptive material" to the error correction methods of claims 18 and 23.

Claims 19, 24, 37 and 38 fail to recite any positive limitation further limiting the error correction methods of claims 18 and 23. Claims 19, 24, 37 and 38 instead recite the intended use of the error correction methods of claims 18 and 23 on data comprising sync data without reciting any positive limitation in the form of a step describing how the sync data is used further narrowing the error correction methods of claims 18 and 23.

Claims 28 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements.

Claims 28 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claims 28 and 33 recite, "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block". While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function, because apparatus claims cover what a device is, not what a device does (Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)).

The previous quoted recitation is "nonfunctional descriptive material" describing a data structure used in the data storage environment for which the error correction apparatus of claims 28 and 33 is intended to be applicable. Claims 28 and 33 fail to recite any structural element and/or structural interconnections explicitly relating the quoted "nonfunctional descriptive material" to the error correction apparatus of claims 28 and 33.

Claim Rejections - 35 USC § 102/103

Where applicant claims a composition in terms of a function, property or characteristic and the composition of the prior art is the same as that of the claim but the function is not explicitly disclosed by the reference, the examiner may make a rejection under both 35 U.S.C. 102 and 103, expressed as a 102/103 rejection. "There is nothing inconsistent in concurrent rejections for obviousness under 35 U.S.C. 103 and for anticipation under 35 U.S.C. 102." In re Best, 562 F.2d 1252, 1255 n.4, 195 USPQ 430, 433 n.4 (CCPA 1977). This same rationale should also apply to product, apparatus, and process claims claimed in terms of function, property or characteristic. Therefore, a 35 U.S.C. 102/103 rejection is appropriate for these types of claims as well as for composition claims.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

> applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 17, 19, 20, 22, 24, 25, 27, 29, 30, 32, 34 and 35 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Marchant; Alan B. (US 6631492 B2) and Kobayashi; Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi).

35 U.S.C. 102(e) rejection of claims 17, 22, 27 and 32.

Marchant teaches an error correction method using a plurality of pieces of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of inner/row codeword sub

data which comprise error correction codes that are independent from error correction codes of an outer/column error correction target code line to configure erasure position information; Note: col. 3 ,lines 41-57 in Marchant teaches that inner/row codeword sub data of the product code is used to configure erasure position information), said method comprising: judging whether or not a first piece of data, which is one of a plurality of pieces of data of the error correction target code line, and a second piece of data, which is one of a plurality of pieces of data of a previous error correction code line, were located between the same pieces of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of data of the outer/column error correction target code line 44b, and a second piece of data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of data of a previous error correction code line 44a, were located between the same pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving); configuring erasure position information of said first piece of data belonging to the error correction target code line to be the same as identical to erasure position information of said second piece of data belonging to the previous error correction code line when said judgment step judging judges that the first piece of data and the second piece of data are both located between the same pieces of sub data (col. 6, lines 28-56 in Marchant teach that symbols in a scratch field are configured/flagged with erasure information for a scratch so that they are configured/flagged with erasure position information for the same scratch, in particular; this process is a step for configuring/flagging erasure

position information of said first piece of data 48b belonging to the outer/column error correction target code line 44b to be the same as identical row position 3 to erasure position information of said second piece of data 48a belonging to the previous error correction code line 44a when said judgment step judging judges that the first piece of data 48b and the second piece of data 48a are both located between the same pieces of inner/row codeword sub data rows 2 to 4); and performing error correction on the error correction target code line (col. 6, lines 28-56 in Marchant).

Note: col. 6, lines 28-56 in Marchant teach that scratch detetection is performed prior to ECC. Col. 4, lines 41-60 in Marchant teach cross interleaved codes such as in U.S. Pat. No. 5,841,794 and Figure 3B teaches that de-interleaving for cross interleaved codes takes place after inner code decoding, that is, after ECC correction starts, hence; Marchant teaches an embodiment where scratch detection takes place before de-interleaving on read Cross-interleaved ECC encoded data.

As per claim 22, only data in the scratch region of Figure 7 are subjected to erasure error detection. Other ECC codewords not lying in the scratch region are ECC decoded.

As per claim 27, claim 27 recites an apparatus with the same limitations as in claim 17.

As per claim 32, claim 32 recites an apparatus with the same limitations as in claim 22.

Furthermore; col. 5, lines 40-42 and col. 4, lines 42-44 in Marchant teaches the use of ECC cross-interleaved product codes. Col. 6, lines 28-50 in Marchant teaches that scratch detection is performed and erasures are flagged before ECC processing to decode the ECC code takes place.

Figure 7B of the Kobayashi teaching reference teaches that Erasure flagging is performed in AZD unit 10 prior to decoding a ECC cross-interleaved product codes and prior to de-interleaving.

35 U.S.C. 102(e) rejection of claims 19, 24, 29 and 34.

Sub data 48a and 48b in Figure 7 of Marchant is sync data for configuring/flagging erasures.

35 U.S.C. 102(e) rejection of claims 20, 25, 30 and 35.

If first data is outside of sub data 48a and 48b in Figured 7 of marchant.

Claims 18, 23, 28, 33 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant; Alan B. (US 6631492 B2) and Kobayashi; Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi) in view of Shutoku; Toshiyuki et al. (US 7089401 B2, hereafter referred to as Shutoku).

35 U.S.C. 103(a) rejection of claims 18, 23, 28 and 33.

Marchant teaches an error correction method using a plurality of pieces of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information (col. 3, lines 30-59 in Marchant teaches using a plurality of pieces of inner/row codeword sub data which comprise error correction codes that are independent from error correction

codes of an outer/column error correction target code line to configure erasure position information; Note: col. 3 ,lines 41-57 in Marchant teaches that inner/row codeword sub data of the product code is used to configure erasure position information), said method comprising: judging whether or not a first piece of data, which is one of a plurality of pieces of data of the error correction target code line, and a second piece of data, which is one of a plurality of pieces of data of a previous error correction code line, were located between the same pieces of sub data before being deinterleaved (col. 6, lines 28-56 in Marchant teach judging whether or not a first piece of data 48b in inner/row codeword sub data row 3 of Figure 7, which is one of a plurality of pieces of data of the outer/column error correction target code line 44b, and a second piece of data 48a in inner/row codeword sub data row 3, which is one of a plurality of pieces of data of a previous error correction code line 44a, were located between the same pieces of inner/row codeword sub data rows 2 to 4 before being deinterleaving); configuring erasure position information of said first piece of data belonging to the error correction target code line to be the same as identical to erasure position information of said second piece of data belonging to the previous error correction code line when said judgment step judging judges that the first piece of data and the second piece of data are both located between the same pieces of sub data (col. 6, lines 28-56 in Marchant teach that symbols in a scratch field are configured/flagged with erasure information for a scratch so that they are configured/flagged with erasure position information for the same scratch, in particular; this process is a step for configuring/flagging erasure position information of said first piece of data 48b belonging to the outer/column error

correction target code line 44b to be the same as identical row position 3 to erasure position information of said second piece of data 48a belonging to the previous error correction code line 44a when said judgment step judging judges that the first piece of data 48b and the second piece of data 48a are both located between the same pieces of inner/row codeword sub data rows 2 to 4); and performing error correction on the error correction target code line (col. 6, lines 28-56 in Marchant).

Note: col. 6, lines 28-56 in Marchant teach that scratch detetection is performed prior to ECC. Col. 4, lines 41-60 in Marchant teach cross interleaved codes such as in U.S. Pat. No. 5,841,794 and Figure 3B teaches that de-interleaving for cross interleaved codes takes place after inner code decoding, that is, after ECC correction starts, hence; Marchant teaches an embodiment where scratch detection takes place before de-interleaving on read Cross-interleaved ECC encoded data.

As per claim 23, only data in the scratch region of Figure 7 are subjected to erasure error detection. Other ECC codewords not lying in the scratch region are ECC decoded.

As per claim 28, claim 28 recites an apparatus with the same limitations as in claim 18.

As per claim 33, claim 33 recites an apparatus with the same limitations as in claim 23.

Furthermore; col. 5, lines 40-42 and col. 4, lines 42-44 in Marchant teaches the use of ECC cross-interleaved product codes. Col. 6, lines 28-50 in Marchant teaches that scratch detection is performed and erasures are flagged before ECC processing to decode the ECC code takes place.

Figure 7B of the Kobayashi teaching reference teaches that Erasure flagging is performed in AZD unit 10 prior to decoding a ECC cross-interleaved product codes and prior to de-interleaving.

However Marchant does not explicitly teach the specific use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block".

Shutoku, in an analogous art, teaches use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code

line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block" (Figure 1-3 and col. 8, lines 52-55 in Shutoku).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Shutoku by including use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub

data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block". This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a typical DVD recording data structure as encompassed in the language "wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error

correction target code line extends so as to be located in both of the first and second main data areas of the ECC block" would have provided scratch protection for DVDs.

35 U.S.C. 102(e) rejection of claims 37-40.

Sub data 48a and 48b in Figure 7 of Marchant is sync data for configuring/flagging erasures.

1. Claims 21, 26, 31 and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Marchant; Alan B. (US 6631492 B2) and Kobayashi; Hisashi et al. (US 6029264 A, hereafter referred to as Kobayashi) in view of Eachus; Joseph J. (US 3685016 A).

35 U.S.C. 103(a) rejection of claims 21, 26, 31 and 36.

Marchant substantially teaches the claimed invention described in claims 17-20, 22-25, 27-30 and 32-35 (as rejected above).

However Marchant does not explicitly teach the specific use of avoiding error correction when error correction capabilities are exceeded.

Eachus, in an analogous art, teaches use of avoiding error correction when error correction capabilities are exceeded (col. 13, lines 1-10 in Eachus).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Marchant with the teachings of Eachus by including use of avoiding error correction when error correction capabilities are exceeded. This modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that use of avoiding error correction when error correction capabilities are exceeded would have provided means for avoiding meaningless calculations (col. 13, lines 1-10 in Eachus).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joseph D. Torres
Primary Examiner
Art Unit 2112

/Joseph D. Torres/
Primary Examiner, Art Unit 2112